Push/Pull Class-DE Switching Power Amplifier

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Abstract — **The new class-DE of switching amplifiers is described. It combines the advantages of a push/pull class-D topology with some peculiarities of class-E operating, which allows to exclude switching power losses. Transistors in a class-DE amplifier operate with underlappings, during which their shunt capacitances are recharged. Therefore it is possible to maintain high drain efficiency on higher frequencies, that is the operating frequency may be two to three times as large as in a push/pull class-D amplifier.**

I. Introduction

Push/pull class-D switching power amplifiers with an output resonance circuit are known to transform the power consumed from the supply into that at the fundamental frequency without power losses at higher harmonics in an additional ballast [1, 2]. Class-D amplifiers with a series-resonant circuit have a number of certain advantages as compared with those with a parallel-resonant circuit. In such amplifiers the peak factor of the drain (collector) voltage does not exceed 2 (against π with a parallel-resonant circuit), which provides essentially higher output power levels under a given limitation for the maximum drain-to-source (collector-to-emitter) voltage. The drain (collector) current waveform in a class-D amplifier with a series-resonant circuit is half-sinusoidal, thus being much easier to provide than the square current waveform with a parallel-resonant circuit. Lastly, only this kind of switching amplifiers due to the low equivalent output impedance is used when building summators of two PM waves in LINC technique.

Frequency limitations for the referred amplifier are first of all conditioned by the transistor output shunt capacitances, which cause additional switching power losses. In this paper the new class-DE of push/pull power amplifiers is described. The switching power losses are completely excluded in this class, and the advantages of a push/pull class-D amplifier with a series-resonant circuit over a class-E amplifier (peak factor of the output voltage no more than 2, suppression of the even harmonics at the load) are maintained.

The idea of complete excluding the switching power losses in a push/pull class-D amplifier was stated in [3]. To this end the amplifier, unlike class-D, operates with underlappings, that is each of transistors is on for less than half period. Thus, there are two intervals of time in a period, when both transistors are simultaneously off, and during these intervals of underlapping the shunt capacitances are recharged by the load current from 0 to V_{max} or from V_{max} to 0. Thereby each transistor is turned on under its output voltage $V_{out} \approx 0$, and, hence, the switching power losses are absent. To achieve zero voltage switching (ZVS) conditions it is necessary to add a supplementary inductance in series with the resonance circuit. During the intervals of underlapping a transient takes place in the circuit consisting of the supplementary inductance and the summary shunt capacitance of two transistors. That is similar to class-E, but occurs twice a period.

As it can be seen, the reported amplifier combines the peculiarities of a push/pull class-D amplifier and those of a class-E amplifier, and since that it is called class-DE amplifier.

In [3] analysis of the referred amplifier was performed with the following assumptions: the shunt capacitances of the transistors are constant and do not depend upon the output voltages; power dissipation in the transistors takes place only when they are on. In the present paper a detailed analysis of class-DE is performed, and, unlike [3], the non-linear character of the shunt capacitances and the power losses in an off transistor are taken into account.

II. Current And Voltage Waveforms

The equivalent circuit of a class-DE amplifier is shown in Fig.1. The L_2C-series-resonance circuit is tuned at the fundamental frequency f_0. With the loaded quality factor (Q) of the resonance circuit being $Q > 3..5$, the current through the load is nearly harmonic: $I_{load} = I_{max}\sin(\tau)$, where the phase angle τ is $\omega_0 t$, and ω_0 is $2\pi f_0$. The supplementary inductance L_1 is added in series with the resonance circuit to obtain ZVS conditions. Under that I_{load} can be considered to be harmonic as before since, firstly, the $(L_1 + L_2)C$-circuit is insignificantly detuned from the operating frequency f_0, and, secondly, due to symmetry in the cirquit there is no second harmonic in the V_{ds} spectrum, and the third harmonic of V_{ds} is more than three times as low as the fundamental.

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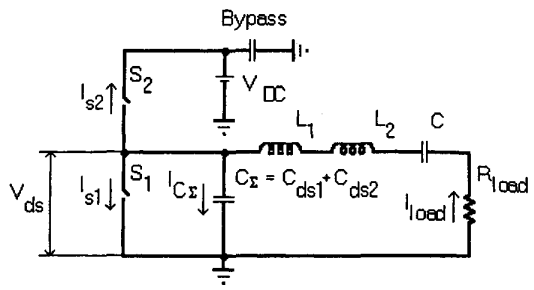

Fig.1. Equivalent circuit of the class-DE amplifier.

The output shunt capacitance of a MOSFET is a function of the drain-to-source voltage:

$$C_{ds} \approx C_V \sqrt{\frac{V_{DC}}{2V_{ds}}}, \quad (1)$$

where C_V is the shunt capacitance value under the average drain-to-source voltage $V_{ds} = V_{DC}/2$, and V_{DC} is the supply voltage.

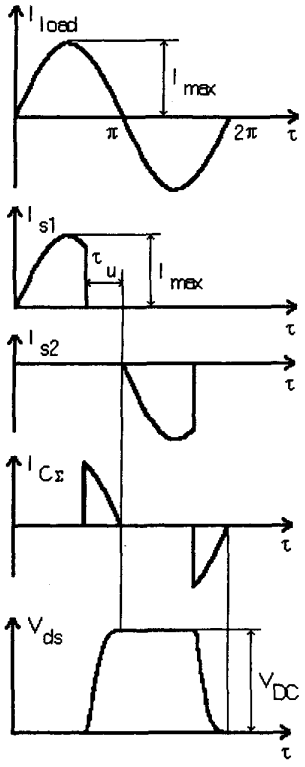

Fig. 2. Waveforms of class-DE.

According to Fig.1, the voltage across Switch 1 is V_{ds}, and that across Switch 2 is $V_{DC} - V_{ds}$. Therefore the summary shunt capacitance can be presented as follows:

$$C_\Sigma = C_{ds1} + C_{ds2} \approx C_V \left(\sqrt{\frac{V_{DC}}{2V_{ds}}} + \sqrt{\frac{V_{DC}}{2(V_{DC} - V_{ds})}} \right). \quad (2)$$

The waveforms of class-DE are shown in Fig. 2. During the interval $0 < \tau \le \pi - \tau_u$, where τ_u is the interval of underlapping, Switch 1 is short circuited, and Switch 2 is open circuited:

$$I_{s1} = I_{load}, I_{s2} = 0, I_{C\Sigma} = 0, V_{ds} = 0.$$

During the interval $\pi < \tau \le 2\pi - \tau_u$ Switch 1 is open circuited, and Switch 2 is short circuited:

$$I_{s1} = 0, I_{s2} = I_{load}, I_{C\Sigma} = 0, V_{ds} = V_{DC}.$$

During the intervals $\pi - \tau_u < \tau \le \pi$ and $2\pi - \tau_u < \tau \le 2\pi$ both switches are open circuited:

$$I_{s1} = 0, I_{s2} = 0, I_{C\Sigma} = I_{load}.$$

The voltage V_{ds} is bound with the current $I_{C\Sigma}$ by a first order differential equation $\omega_0 C_\Sigma dV_{ds}/d\tau = I_{C\Sigma}$, or

$$\omega_0 C_V \sqrt{\frac{V_{DC}}{2}} \left(\frac{1}{\sqrt{V_{ds}}} - \frac{1}{\sqrt{V_{DC} - V_{ds}}} \right) \frac{dV_{ds}}{d\tau} = I_{max} \sin\tau. \quad (3)$$

Solving (3) with the initial condition $V_{ds}(\pi - \tau_u) = 0$ for $\pi - \tau_u < \tau \le \pi$ and with the initial condition $V_{ds}(2\pi - \tau_u) = V_{DC}$ for $2\pi - \tau_u < \tau \le 2\pi$, we obtain:

$$V_{ds} = \frac{V_{DC}}{2} \left[1 \mp \frac{1 + \cos\tau_u \pm 2\cos\tau}{(1 - \cos\tau_u)^2} \times \right.$$
$$\left. \times \sqrt{2(1 - \cos\tau_u)^2 - (1 + \cos\tau_u \pm 2\cos\tau)^2} \right], \quad (4)$$

where the upper symbol is for the interval $\pi - \tau_u < \tau \le \pi$, the lower one is for the interval $2\pi - \tau_u < \tau \le 2\pi$, and

$$\tau_u = \arccos\left(1 - \frac{2\sqrt{2}\omega_0 C_V V_{DC}}{I_{max}} \right). \quad (5)$$

The V_{ds} waveform on the intervals of underlapping (4) differs from obtained in [3] in assumption of the constant output capacitances (not depicted in Fig. 1, for its scale is rather small). With non-linear C_Σ growth (or fall) of V_{ds} delays at first, and then accelerates notably.

The equations for voltage and currents obtained in the recent section completely describe the state of the amplifier's output circuit. Yet for the amplifier design it is necessary to know some parameters of the state, which are considered in the next section.

III. ZVS Parameters

To achieve ZVS conditions it is necessary to provide a

certain value of the underlapping interval τ_u, and a certain relationship between C_V, L_1 and R_{load} is to be established as well. These values are considered in the recent section.

The first harmonic of the voltage V_{ds} consists of two components: the resistance voltage across R_{load} and the reactive voltage across L_1. The magnitudes of the two components are determined by Fourier transform:

$$U_{load} = \left| \frac{1}{\pi} \int_{\pi-\tau_u}^{2\pi} V_{ds} \sin\tau \, d\tau \right|, \quad U_L = \left| \frac{1}{\pi} \int_{\pi-\tau_u}^{2\pi} V_{ds} \cos\tau \, d\tau \right|. \quad (6)$$

For U_{load} an analytical expression was found:

$$U_{load} = \frac{V_{DC}}{\pi}(1+\cos\tau_u), \quad (7)$$

and for U_L, as it turned out, only a numerical solution exists. Taking into consideration that $R_{load} = U_{load}/I_{max}$, from (5) and (7) we find an expression for the normalized admittance of the summary shunt capacitance:

$$c = \omega_0 C_V R_{load} = \frac{1}{2\sqrt{2}\pi} \sin^2\tau_u. \quad (8)$$

The expression for the normalized impedance of the inductance L_1 becomes clear from the equivalent circuit in Fig. 1:

$$l = \frac{\omega_0 L_1}{R_{load}} = \frac{U_L}{U_{load}}. \quad (9)$$

Fig. 3 shows the coefficients l and c as functions of τ_u. As compared with the results in [3] (shown in dash line in Fig. 3), the nonlinearity of the output capacitances does not affect the value of l, and c is $\sqrt{2}$ times as small as in case of the constant capacitances.

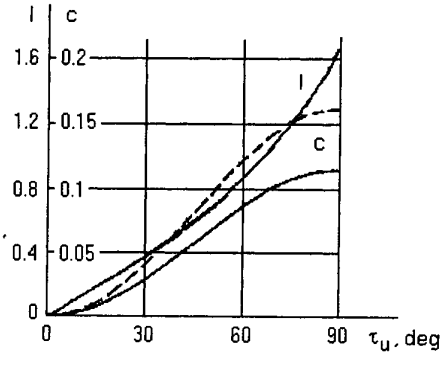

Fig. 3. Coefficients l and c in funtion of τ_u.

Since $U_{load} = 2P_{load}/I_{max}$, where P_{load} is the power in R_{load}, from (5) and (7) a formula for τ_u, which, unlike (5), contains only parameters set on design, can be obtained:

$$\tau_u = \arccos\left(\frac{\pi P_{load} - \sqrt{2}\omega_0 C_V V_{DC}}{\pi P_{load} + \sqrt{2}\omega_0 C_V V_{DC}} \right). \quad (10)$$

Comparison with the analogous dependence obtained in [3] shows that under given ω_0, V_{DC}, C_V, and P_{load} the nonlinearity of the shunt capacitances leads to the 10..15 % increase of τ_u value, needful to provide ZVS, and this divergence is higher for the lesser τ_u values.

When designing the amplifier, one should also determine the peak factors of the output voltage and current. The peak factor of V_{ds} is 2 since $V_{ds\,max} = V_{DC}$, and the average value of V_{ds} is $V_{DC}/2$. The peak factor of the drain current depends upon τ_u. Since the current of the transistor shunt capacitance does not contain a dc component, the dc component I_{d0} of the drain current is determined by I_{s1} (or I_{s2}) waveform:

$$I_{d0} = \frac{1}{2\pi} \int_0^{\pi-\tau_u} I_{s1} \, d\tau = \frac{I_{max}}{2\pi}(1+\cos\tau_u). \quad (11)$$

The peak factor then is

$$p_I = \frac{I_{max}}{I_{d0}} = \frac{2\pi}{(1+\cos\tau_u)}. \quad (12)$$

Thus, all the parameters, that are necessary for the output circuit design, have been described.

IV. Maximum Operating Frequency Of A Class-DE Amplifier

One of the causes for the limitation of the maximum operating frequency of a class-DE amplifier is the value of the transistor shunt capacitance. To raise f_0 under given V_{DC}, C_V, and P_{load} it is necessary to enlarge τ_u (see (10)). However, with enlarging τ_u the peak factor of the drain current increases (12). Besides that, due to the non-zero resistance of an on transistor and the power losses in the parasitic drain and source resistances on the intervals, when the current flows through the shunt capacitances, enlarging τ_u leads to the increase of the power dissipated in the transistors and to the decrease of the drain efficiency. For that reason some limitations for the maximum value of $\tau_u = \tau_{u\,max}$ do exist, so that further enlarging τ_u with a view to raise the operating frequency becomes inexpedient or even inadmissible, and transistors with a lower C_V are to be used. Presenting (10) as

$$f_{0\,max} = \frac{P_{load}}{2\sqrt{2}C_V V_{DC}^2} \cdot \frac{1-\cos\tau_{u\,max}}{1+\cos\tau_{u\,max}}, \quad (13)$$

we obtain the equation for the maximum output frequency, at which ZVS can be achieved under the known limit of $\tau_u = \tau_{u\,max}$. Note, that, according to (13), with $\tau_{u\,max} \to 0$ and $C_V \neq 0$ $f_{0\,max} \to 0$. That means that in this case ZVS cannot be achieved at any $f_0 > 0$. When enlarging τ_u from 0 to the given $\tau_{u\,max}$ under fixed V_{DC}, C_V and P_{load}, the operating frequency in class-DE changes from 0 to $f_{0\,max}$. Under the fixed $\tau_{u\,max}$ the maximum frequency can be raised by increasing P_{load}; increasing V_{DC} or C_V will result in $f_{0\,max}$ decrease.

V. Drain Efficiency

When analysing energetic characteristics of the output circuit, not only the power losses in an on transistor due to its non-zero resistance, but also the additional power losses on the intervals of underlapping, when the transistors are off, but the current flows through their shunt capacitances and, hence, through the parasitic drain and source resistances, were taken into account, unlike [3]. Because of the lack of space we adduce here only the resultant formula for the drain efficiency:

$$\eta \approx \frac{1}{2} + \frac{1}{2}\sqrt{1 - \frac{2p_1^2 P_{load} r}{V_{DC}^2}}, \qquad (14)$$

where r is the parasitic resistance of an on transistor. Since p_1 is a function of τ_u (12), it is obvious that η decreases with enlarging τ_u. Moreover, the larger is τ_u, the higher is the ratio between the power dissipated in the off transistors and that in the on ones.

VI. Simulation

To verify the results of the theoretic analysis, simulation in Micro-CAP 6.2 was carried out. An amplifier built upon IRFP440 500 V, 8.8 A (C_{ds} = 310 pF under V_{ds} = 25 V) MOSFETs was investigated. P_{load} = 400 W and V_{DC} = 200 V were set on design. The design was accomplished for a number of operating frequencies in 0.5..8 MHz range. The loaded quality factor Q = 4 of the resonance circuit was provided. The driving waveforms were sinusoidal, and the required τ_u at each frequency was set by varying the gate bias. At the same time an analogous push/pull class-D amplifier was simulated in comparison.

Fig. 4 shows simulated drain efficiency of class-DE and class-D amplifiers as a function of operating frequency. Theoretic dependencies are depicted in continuous line. As with raising frequency the value of τ_u increases in class-DE (from 17° at 0.5 MHz to 61° at 8 MHz), the relative magnitude of the first harmonic of the drain current spectrum decreases. Under constant output power that leads to the increase of the drain current peak value (from 6.7 A at 0.5 MHz to 8.8 A at 8 MHz). Therefore the dissipated power increases, and the drain efficiency degrades. Yet up to 8 MHz efficiency exceeds 90 %. In class-D degradation of efficiency is in the main conditioned by the switching power losses, which are proportional to the operating frequency. Comparison of experimental data for the two classes shows that class-DE operating gives sufficient gain in drain efficiency, and, therefore, frequency range can be 2..3 times as wide as in class-D.

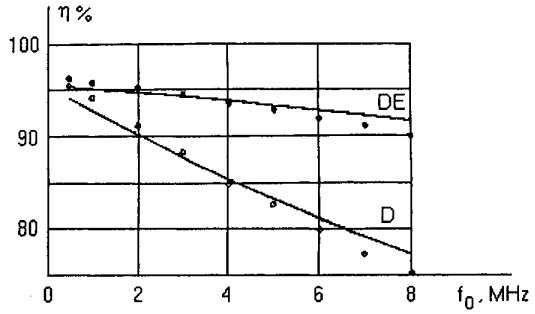

Fig. 4. Simulated drain efficiency vs. operating frequency (tokens) and theoretic dependencies (continuous line).

VII. Conclusion

Analysis of the push/pull class-DE amplifier has been performed with the nonlinearity of the shunt capacitances and the power dissipation in an off transistor taken into account. ZVS parameters and the frequency limitation conditioned by the shunt capacitances have been determined. It has been shown that the nonlinearity of the capacitances has sufficient influence upon some parameters of the amplifier.

Theoretic analysis and simulation show that transition from class-D to class-DE allows to operate at frequencies 2..3 times as high as in class-D with maintaning the advantages of a push/pull class-D amplifier over a class-E amplifier.

References

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